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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/734,704	12/13/2000	Kenji OI	1076.1059/JDH	3349

21171 7590 09/09/2004

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EXAMINER	
DANG, KHANH NMN	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/734,704	OI ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2004*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 1, 33-36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, line 10, "the analysis circuit" lacks antecedent basis. Further, it is unclear what may be the relationship(s) between such a circuit and other structural elements recited in the claim.

In claim 33, a "predetermined connection procedure" has not been properly defined in the claims. It is unclear from the current language of the claim what may be the relationship(s) between the so-called "self-diagnosis method" and "predetermined connection procedure." In line 6, "the received data" lacks clear antecedent basis.

In claim 35, the phrase, "a data signal whose waveform is same as that of data used during an actual non-test data transfer" renders the claim indefinite, since the "data used during actual non-test data transfer" and its "waveform" have not been properly defined or recited positively in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Ikegawa.

At the outset, it is first noted that similar claims will be grouped together to avoid repetition in explanation.

As broadly drafted, these claims do not define any structure/step that differs from Ikegawa. With regard to claims 1, 2, 5, 9, and 10, Ikegawa discloses an interface (IEEE 1394 interface) having a plug and play function and connected to a host controller (101, for example), wherein the interface (IEEE1394 interface) performs a predetermined bus reset sequence (also "reset sequence" in Ikegawa) in response to a bus reset generated by the plug and play function (when a new I/O device is added or removed from the 1394 bus) in accordance with a change in the status of an external bus, the interface (1394) comprising: an analysis circuit for analyzing data provided from the external bus during the bus reset sequence and for determining whether the bus reset sequence has

been completed normally, wherein the analysis circuit provides the data to the host controller when the bus reset sequence has been completed normally. In Ikegawa, the 1394 serial bus corresponds to "Plug and Play", it automatically recognizes a device connected to the cable for the 1394 interface, thus recognizes connection status. When a device is removed from the interface, or a new device is added to the interface, the bus is automatically reset. The respective devices (nodes) connected to the 1394 interface/bus are provided with a node ID and are recognized as nodes constructing the network. The detection of change of network construction is made by detecting change of bias voltage at the connector port, or in another word, change in current characteristics since voltage and current are closely related. When adding/removing devices (nodes) or power ON/OFF, the network construction changes and it is necessary to recognize a new network construction by the host controller, the respective devices (nodes) detect the change of network construction, send a bus reset signal onto the bus, and send the necessary data to the host controller after the reset sequence is completed without error (or in another word, completed normally) so that the network is able to recognize the new network construction. When the reset signal is sent from one node, the physical layer of the respective nodes receives the bus reset signal, and at the same time, notifies the link layer of the occurrence of bus reset, and forwards the bus reset signal to the other nodes. When all the nodes have received the bus reset signal, a bus reset sequence is started. Thus, it is clear that the Bus Management (Fig. 7) or a so-called "analysis circuit" manages/analyzes the connection status data (obtained

from, for example, adding/removing devices), and IDs of the respective device connected to the 1394 bus; and send the necessary data to the host controller only after the bus reset sequence is completed normally. No data transfer occurs during the bus reset sequence. With regard to claims 3 and 4, the Bus Management (Fig. 7) or a so-called "analysis circuit" generates the bus reset/reset sequence upon detecting an abnormality (also "abnormality" in Ikegawa) of the data (connection status data obtained from, for example, adding/removing devices (nodes)) during the data analysis. With regard to claims 6-8, it is clearly inherent that the 1394 interface system of Ikegawa must have a storage means (buffers/registers) to temporarily store/analyze the ID/data during reset sequence so that the necessary data can be provided to the host controller after the reset sequence is successfully completed. With regard to claim 11, the interface system of Ikegawa further comprises a port circuit (associated with the connector port, Fig. 7) for detecting the status of the external bus and generating associated detection information; a physical layer circuit (associated with the physical layer, Fig. 7) connected to the port circuit to receive the data via the port circuit and generate a data packet; a link layer circuit (associated with the link layer, Fig. 7) connected to the physical layer circuit to determine whether the data packet is addressed to the interface system; and a buffer memory (see also discussion above regarding claims 6-8) connected to the link layer circuit to store the detection information and the data packet which are provided via the port circuit, the physical layer circuit, and the link layer circuit, wherein the bus management (Fig. 7) or a so-called "analysis circuit"

connected to the port circuit (associated with the connector port, Fig. 7) to analyze the detection information, and to the physical layer circuit (associated with the physical layer, Fig. 7) to analyze the data packet provided during the bus reset sequence and to determine whether the data packet is normal (see also discussion above regarding claim 2). With regard to claim 12, since the IEEE 1394 interface of Ikegawa has to conform with the IEEE 1394 specification, it is clearly inherent that the ID/data packet of/from a respective devices (node) must be compared with a so-called "predetermined sequence information" or bits and "predetermined data packet" both typically stored in a memory so that the respective device can be recognized by the host/bus when added or removed from the 1394 bus. If the results are validated, the so-called "analysis circuit" or bus management will provide the necessary data to the host controller after a normally completed bus reset sequence. See also discussion above regarding claim 2). With regard to claims 13-23, see at least discussion regarding claims 1-12 above. Note also that in Ikegawa, analyzing/managing the 1394 interface involving bus reset/reset sequence is a form of "self-diagnosis." With regard to claims 24-31, one using the 1394 interface system of Ikegawa would have performed the same steps set forth in claims 24-31.

Response to Arguments

Applicants' arguments filed 7/12/2004 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997)*. In fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.*, 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

The 112 2ND Paragraph Rejection:

Applicants' amendments to claims 33 and 35 do not overcome the rejection under 35 USC 112, 2nd paragraph. Further, Applicants do not provide any reason as to why the amendment should overcome the rejections.

The Ikegawa 102(e) Rejection:

With regard to claims 1 (with claims 2-12 stand or fall together) and new claim 32, Applicants argued that Ikegawa does not disclose or suggest

"analyzing bus reset sequence data, including ID packet" and providing the "bus reset sequence data to the host controller when determined that the bus reset sequence has been completed normally." It is first noted that any 1394 device must be in full compliance with the 1394 specification. Further, contrary to Applicants' argument, in Ikegawa, the 1394 serial bus corresponds to "Plug and Play", it automatically recognizes a device connected to the cable for the 1394 interface, thus recognizes connection status. When a device is removed from the interface, or a new device is added to the interface, the bus is automatically reset. The respective devices (nodes) connected to the 1394 interface/bus are provided with a node ID and are recognized as nodes constructing the network. When adding/removing devices (nodes) or power ON/OFF, the network construction changes and it is necessary to recognize a new network construction by the host controller, the respective devices (nodes) detect the change of network construction, send a bus reset signal onto the bus, and send the necessary data to the host controller after the reset sequence is completed without error or in another word, completed normally so that the network is able to recognize the new network construction. When the reset signal is sent from one node, the physical layer of the respective nodes receives the bus reset signal, and at the same time, notifies the link layer of the occurrence of bus reset, and forwards the bus reset signal to the other nodes. When all the nodes have received the bus reset signal, a bus reset sequence is started. Thus, it is clear that the Bus Management (Fig. 7) or a so-called "analysis circuit" manages/analyzes the connection status data (obtained from, for example,

adding/removing devices), and IDs of the respective device connected to the 1394 bus; and send the necessary data to the host controller only after the bus reset sequence is completed without error or "normally." No data transfer occurs during the bus reset sequence. It is the very nature of 1394 bus that a network must be configured before data transfer. Specifically, all nodes (including newly added or removed nodes) must be accounted for in order to configure a network. Otherwise, the network will have to be reset and until the reset is completed without error or "normally" data will not be able to transfer. Further, the 1394 bus always performs arbitration of a bus-used right prior to data transfer. Therefore, unless all nodes (including newly added or removed nodes) are accounted for after a completed reset there will be no arbitration and as a consequence, no data transfer. In other words, it has to be determined whether a completed reset is "normal" or without error (a completed reset is considered "normal" when all nodes are successfully accounted for, a crucial step before configuring any updated network based on the current status of all connected nodes) before arbitration and subsequently, data transfer. Further, any 1394 device must be in full compliance with the 1394 specification. Therefore, in Ikegawa, IDs of the respective node connected to the 1394 bus must be analyzed during bus reset according to the 1394 specification. See Short Introduction into IEEE 1394, Bus Reset; and IEEE Standard 1394a, cited below.

With regard to claim 13 (with claims 14-31 and new claims 33-36 stand or fall together), Applicants argued that Ikegewa does not disclose "a self-diagnosis circuit for performing self-diagnosis of the interface prior to the predetermined

connection procedure, wherein the interface suspends transition to the predetermined connection procedure when the self-diagnosis circuit generates a diagnosis indicating an abnormally of the interface." Contrary to Applicants' argument, in Ikegawa, analyzing/managing the 1394 interface involving bus reset/reset sequence is a form of "self-diagnosis." In other words, the bus management performs a 1394 reset involving checking if there is any change in node connections, any new or removed nodes. In Ikegewa or in any 1394 system, the so-called "self analysis" is only performed during the bus reset prior to the actual connection of a new node to the 1394 bus, for example. Any predetermined network connection procedure obeying 1394 bus specification can be realized only after a reset (or a so-called "self-diagnosis") is completed without error or "normal." It is also clear that a predetermined network connection procedure obeying 1394 bus specification cannot be performed when a reset (or a so-called "self-diagnosis") generates error or "abnormality." Applicants further argue that Ikegewa does not a "transmitting circuit and a receiver circuit." Contrary to Applicants' argument, any IEEE 1394 device including Ikegawa's must be in full compliance with the widely available IEEE 1394 specification. That is the 1394 link layer must include a transmitter and a receiver for data transmission and reception. See also the link layer specified in Applicants' original claim 11 (the link layer is now deleted in currently amended claim 11). It is also clear that data transmitted and received during the 1394 bus reset is self diagnosed to determine if there is any error or abnormality occurred during the 1394 bus reset prior to an actual data connection of a new node to the 1394

network. With regard to claim 24, Applicants argue that Ikegawa does not disclose "connecting the first and second ports to each other prior to the predetermined connection procedure." Contrary to Applicants' argument, any 1394 device including Ikegawa's must be in full compliance with the IEEE 1394 specification. That is the ports/connectors in the physical layer must be first interconnected before any actual connection procedure (adding a new node, for example) so that data can be actually transmitted and received.

"Short Introduction into IEEE 1394, libraw 1394, version 0.9", and "IEEE Standard 1394a, A standard for a High Performance Serial Bus" are cited as relevant art.

Allowable Subject Matter

Claims 35 and 36 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.

Khanh Dang
Primary Examiner